Field-Oriented BLDC Motor Controller with 16 Bit CPU

E523.06

RoHS compliant

Features

- Gate drive circuit for B6-NMOS bridge
- IC supply voltage range 7 to 28V (extended 5V to 42V)
- CPU 16 bit, 24 - 48MHz for application tasks
- 32 kByte FLASH, ECC protected
- 24 kByte Masked ROM
- 4 kByte SRAM, parity protected
- Typical deep-sleep mode current 20µA
- 2nd window watchdog and two independent clocks
- LIN2.x, LIN1.3 or bidirectional PWM Interface
- High speed current amplifier for single shunt FOC
- Motor over-current protection with CPU interrupt
- 6 * FET short-circuit protection within gate driver
- Multiplication(16*16bit) & division(32/16bit) modules
- Coprocessor for ADC tasking w/ PWM edge trigger
- ROM library: LIN2.x /1.3 stack routines
- ADC (SAR) 12 bit 1Msample/s
- S&H time programmable down to 167nsec
- 4 channel 16bit PWM generation + 8bit prescaler for left-, right-, center-aligned or free-form toggle PWM
- 4 channel 16bit timer/capture/compare unit
- Clock fine tuning for EMC optimization
- Hardware support for spread spectrum
- Clock adjustment to LIN master possible
- AEC-Q-100 grade 0 qualified (Tamb=150°C)

Applications

- EC, BLDC, PMSM motors 50W to ~1500W
- Cooling fans, HVAC fans, positioning systems
- Fuel, hydraulic, oil and water pumps

General Description

E523.06 is a BLDC motor system-in-a-chip including a 16bit CPU core. It controls 3 NMOS half-bridges for driving BLDC motors, DC motors, or other loads. CPU architecture and motor driver peripherals are optimized for single shunt FOC (Field Oriented Control).

The IC includes a high-speed single shunt foot current measurement and protects against over-current (threshold continuously adjustable), over-temperature, over- and under-voltages and short-circuits (on the fly programmable thresholds for each FET). End-of-line programming is possible via JTAG or high-speed LIN.

Highest performance is provided by a 16bit CPU. A co-processor for ADC tasking automatically collects all analog system information synchronously to the output PWM. These processing units optimize system performance, system reliability, EMC performance, current dissipation and development time. The system clock is tunable in very fine steps to improve EMC behaviour and spread spectrum is supported by on-chip hardware. An adjustment of the system clock of a LIN-master is possible.

The E523.06 is suited for all commutation algorithms such as trapezoid, CZCD (Current Zero-Crossing Detection) and FOC (Field-Oriented Control). Single-shunt FOC is supported by the on-board high speed current amplifier and SARADC co-processor.

Ordering Information

Ordering-No.	Temp Range	Package
E52306A78B	-40°C to +150°C	QFN48L7
E52306A99H	-40°C to +150°C	LQFP48L7EP
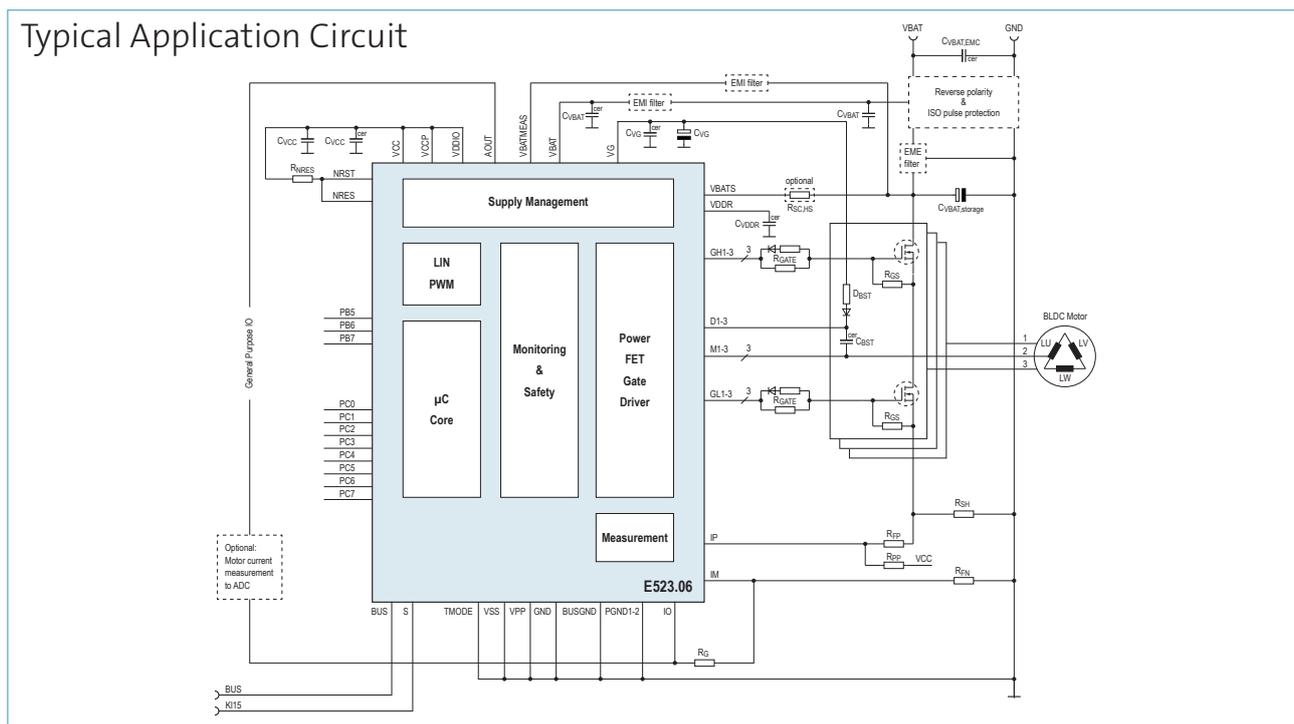
Typical Application Circuit

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